

A 2^7-1 LOW-POWER HALF-RATE 16-GBS CHARGE-MODE PRBS GENERATOR IN 1.2V, 65nm CMOS

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ABSTRACT:

In this work, we propose a half-rate 2^7-1 pseudo random bit sequence (PRBS) generator by employing highly power efficient charge-mode circuit topology at 16-Gb/s. At the target data-rate, proposed charge-mode implementation have the lowest power consumption compared to the traditional current-mode PRBS generator implementations, thanks to the availability of high speed switches in sub-100nm technologies. The proposed charge-mode half-rate PRBS generator is implemented in 1.2 V, 65-nm CMOS technology with a power consumption of 3.35 mW, timing jitter of 0.2 ps and FoM of 0.02-pJ/bit at 16-Gb/s. Thus, the proposed power efficient charge-mode implementation of PRBS generator is an attractive candidate for on-chip bit-error-rate(BER) test and measurement applications.

Keywords: : 2^7-1 PRBS generator, charge-mode logic, half-rate architecture, low-power CMOS, 16-Gb/s, 65-nm CMOS, LFSR, BER testing, BIST, high-speed serial link, and Electronic Design Automation (EDA).

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1.INTRODUCTION

Increasing data-rates in digital circuits and systems has increased the need for high speed test and measurement equipment. However, the cost of this equipment is expensive at high data-rates [1]. Thus, on-chip PRBS generator is a cost-effective solution for testing high-speed digital circuits and systems, especially for network-on-chip (NoC) and off-chip high speed serial link applications. To measure the bit-error-rate (BER), the on-chip PRBS generator acts as a built-in-self-test(BIST) function for test and measurement of these links. Test pattern generation and response verification in on-chip is performed by built-in-self-test(BIST) techniques. A PRBS generator should be capable of generating long sequences

with low power consumption for testing of high speed systems.

Pseudo random binary sequence generator (PRBS generator) is a linear feedback shift register (LFSR) operated with a predefined characteristic polynomial. Early high speed PRBS generators have employed SiGe bipolar [2] and SiGe-BiCMOS [3] technologies for multi-Gb/s applications, since the compound semiconductor technologies have transition frequency (f_T) greater than several 10's of GHz. The speed of the PRBS generator is improved by using active feedback and inductive peaking techniques [4], however, at the cost of increased circuit complexity, area

and power. PRBS generators are designed in sub-clock rate implementations such as half-rate [4] and quarter-rate [5] targeting higher data rates

with low-power consumption. For high data rates, pseudo-random bit sequence patterns must be generated in parallel and then multiplexed [6]. In most of the PRBS generator design works reported to date, current-mode logic (CML) has been the popular choice for designing building blocks such as D flip-flops (DFFs) and EX-OR gates, because of its remarkable performance at high speeds [1]. However, the current-mode logic consumes significant amount of power at high data-rates, making it a power hungry logic [7] and it also suffers from low output voltage swing. On the other hand, voltage-mode logic is not a good choice at high-speeds, even-though its power consumption is less than that of the current-mode logic [8].

In this work, a new charge-mode logic circuit based PRBS generator is proposed and its implementation in 1.2 V, 65-nm CMOS technology is reported. The proposed charge-mode half-rate PRBS generator consumes only 3.35 mW of power, timing jitter 0.2 ps and FOM of 0.02-pJ/bit at 8-Gb/s which is low compared to current mode based PRBS implementations. To the best of authors knowledge, this is the first charge-mode logic based PRBS generator implementations reported to date. Rest of the paper is organized as follows. The architecture of PRBS generator is described in Section II. Section III gives detailed description of the circuits, section IV presents performance results and comparison with the literature. Section V, Concludes the paper.

II. AN INTRODUCTION TO PRBS GENERATOR

A. Pseudo Random Binary Sequences

PRBS generator is designed using a linear feedback shift register (LFSR). LFSR is a shift

register that has an input bit which is a linear function of its previous state. The maximum length sequence (MLS) of $2L-1$ PRBS generator is repeats for every $2L-1$ clock periods except zero state. The random sequence is determined by feedback and position of the EX-OR gates. The position of EX-OR gates is called as tapping and proper tapping is necessary for generation of high speed random sequences [9]. The LFSR locks permanently in all zero state.

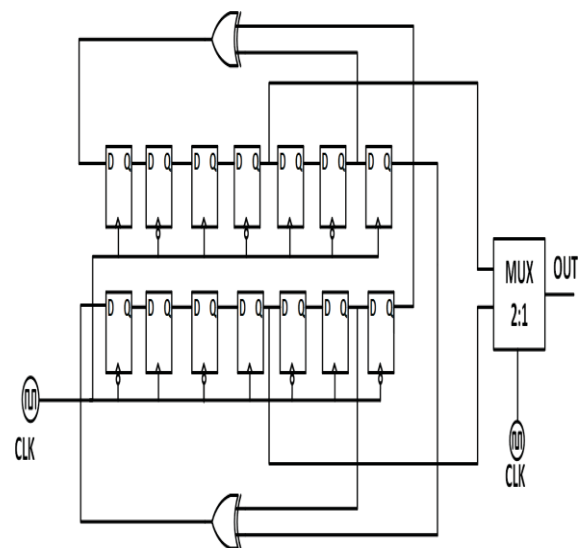


Fig. 1: Interleaved half-rate PRBS generator

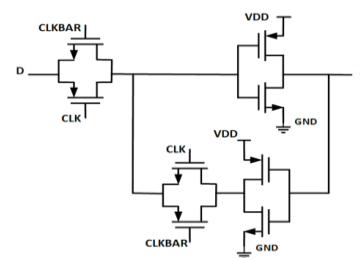


Fig. 2: CMOS charge-mode latch

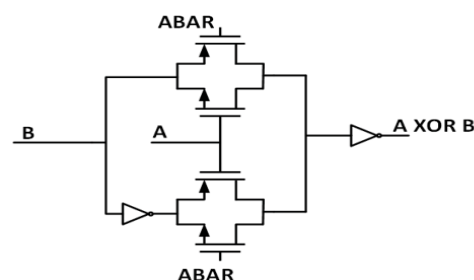


Fig. 3: RMTG EX-OR gate

B. Half-Rate PRBS generator

In this section, a half-rate interleaved PRBS generator architecture is presented as shown in Fig. 1 [4]. The interleaved PRBS generator architecture consists of two parallel full-rate PRBS stages with LFSR and XOR gates. Each LFSR consists of seven latches and it operates at only half-rate clock to generate a full-rate random data. The output sequences of two LFSR stages are uncorrelated and they are separated by a length of $MLS/2$. A multiplexer selects the output of either of the two full-rate PRBS sequence resulting in a high speed data output equal to twice the clock frequency. The two opposite LFSR stages are clocked with inverted clock signals. In interleaved PRBS generator architecture the taps are defined in between the latches unlike the conventional full-rate architecture, where the feedback taps are defined between the flip-flops. The feedback signal is taken from tap 6 of one shift register and tap 7 of the opposite shift register according to the polynomial $P(x) = x^7 + x^6 + 1$.

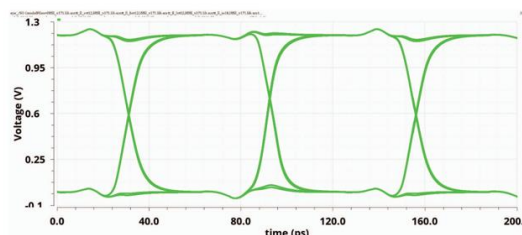


Fig. 4: Eye diagram of proposed half-rate PRBS generator at 16-Gb/s

III. CIRCUIT IMPLEMENTATION

This section presents a brief description and working of the different logic blocks used in proposed charge-mode PRBS generator such as charge-mode D-latch and charge-mode EX-OR gate and multiplexer. The other building blocks such as clock circuitry and buffers are realized with chain of inverters.

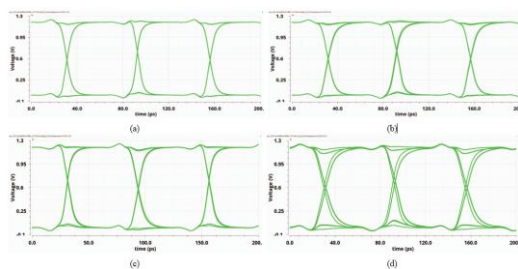


Fig. 5: Eye Diagrams of proposed charge-mode half-rate PRBS generator at 16-Gb/s (a) FF corner (b) SF corner (c) FS corner (d) SS corner

A. Charge-Mode D-Latch

The charge-mode D-latch is designed using the transmission gates and inverters as shown in Fig. 2. The transmission gate approach is used when the power consumption needs to be kept low. The operation of charge-mode D-latch is as follows. When CLK is 'LOW', the forward path transmission gate connects the output to the input. The output Q is 'HIGH', if the input D is 'LOW' initially. When CLK is 'HIGH', the forward path transmission gate is in cutoff region and feedback transmission gate gets switched ON. The transistor's aspect ratios are optimized such that the charge-mode D latch can be operated at 8-Gb/s of data rate with 8-GHz of input clock. The latch is operated at 8-Gb/s and its power consumption is 0.2 mW. The drawback of charge-mode latch is that its driving capability is low, thus buffers are introduced in the feedback path at the input of EX-OR gate.

B. EX-OR gate and multiplexer

The EX-OR gate used in this design is restoring mode transmission gate (RMTG) proposed in [10]. The RMTG EX-OR consists of transmission gates and inverters as shown in Fig. 3. In this work, LFSR, RMTG EX-OR gate and multiplexer [11] are implemented in the charge-mode. The RMTG EX-OR is operated in two modes, of which one is restoring-mode and the other is transmission-mode [10]. When A is logic "HIGH", then B-complement is passed to the output. The 'restoring-path' evaluates output and the input and output are isolated by the static CMOS inverter, which has level restoration capability when A is logic HIGH. The static CMOS inverter provides current driving capability in this mode. When A is logic "LOW", then B is passed to the output. In this case, 'transmission-path' evaluates the output. No level restoring is observed in this case, since the input and output are connected by resistive path because transmission gate lacks its own current driving capability.

IV. PERFORMANCE RESULTS

The circuits are implemented in 1.2 V, 65-nm CMOS technology and simulations are carried out in cadence virtuoso environment. The eye diagram of proposed charge-mode half-rate PRBS generator at 16-Gb/s in typical case is shown in Fig. 4. From Fig. 4, eye-opening of proposed half-rate charge-mode PRBS generator is rail-to-rail and timing jitter of 0.2 ps with amplitude noise of 30 mV. The power consumption of proposed charge-mode half-rate PRBS generator is 3.35 mW at half-rate input clock of 8-GHz. The design is also simulated for process, voltage and temperature (PVT) variations. Charge-mode PRBS generator is simulated in all the five process corners namely, slow-slow(SS), slow-fast(SF), fast-slow(FS), fast-fast(FF) and typical conditions. The charge-mode PRBS generator is simulated for temperature variation from 0°C to 70°C. The PRBS generator is simulated with 10% tolerance in supply voltage, i.e., from 1.1 V to 1.3 V. The proposed charge-mode half-rate PRBS generator is robust to PVT variations across all process corners fast-fast, fast-slow, slow-fast, slow-slow as shown in Fig. 5. The figure-of-merit (FOM) of proposed half-rate charge-mode PRBS generator is 0.02-pJ/bit at 8-GHz half-rate input clock frequency. The layout of proposed charge-mode PRBS generator is shown in Fig. 6 and it occupies an area of 0.002 mm².

Ref	Tech CMOS	Bit-Rate (Gb/s)	Architecture	Output voltage swing	Power (mW)	FOM (pJ/bit)	Result type
This work	65nm	1x16	Half	rail-to-rail	3.35	0.02	simulation
[9]	90nm	1x13	Full	160 mV	222	2.44	simulation
[12]	90nm	1x13.5	Full	250 mV	220	2.33	simulation
[14]	65nm	1x14	Quarter	200 mV	22	-	simulation

TABLE I: Comparison with CMOS based PRBS implementations from literature

1) Comparison with the Literature: The proposed charge-mode half-rate PRBS generator is compared with the CMOS implementations from literature are listed in Table. I. It is evident that the charge-mode PRBS generator is proven to be the low-power

design implementation with rail-to-rail voltage swing.

$$\text{Figure of Merit (FOM)} = \frac{\text{Power}}{\log_2(\text{Length}) * (\text{bit-rate})} \quad (1)$$

The FOM of proposed PRBS generator is 0.02-pJ/b at half-rate input clock of 8-GHz, which is very low when compared to circuit level implementation of PRBS generator in literature at this speed. Lower the FOM, better is the performance of the PRBS generator. Thus, the charge-mode PRBS generator is potential replacement for any CML based PRBS generator reported in literature to date.

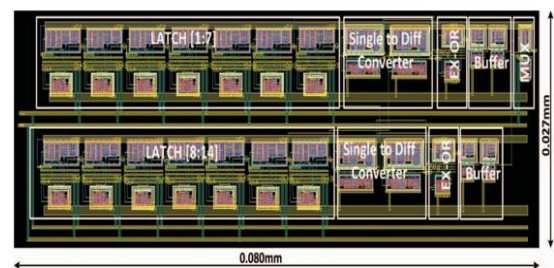


Fig. 6: Layout of charge-mode half-rate PRBS generator

V. CONCLUSION

A 2⁷-1 low-power charge-mode half-rate PRBS generator in

1.2 V, 65-nm CMOS is implemented at 16-Gb/s output data rate. The charge-mode half-rate PRBS generator is designed to operate at high speed with low power consumption by deploying a charge-mode D latch circuit topology. The proposed charge-mode half-rate PRBS generator output data-rate is at 16-Gb/s with 3.35 mW of power consumption at an half-rate clock of 8-GHz. The other key performance parameters such as timing jitter, eye opening and amplitude noise are of values 0.2 ps, 1.2 V and 30 mV respectively. This shows that charge-mode is capable of generating the pseudo random binary sequences with power consumption far better than any CML based PRBS generator. The PRBS generator is also simulated for process, voltage and temperature variations. The design shows robust performance over all the corners. Thus, the proposed charge-mode PRBS generator is a potential candidate for low-power high-speed

on-chip testing applications including testing of clock-and- data recovery (CDR) circuits where longer patterns are required.

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