

LOW-POWER FPGA IMPLEMENTATION OF A SINGLE-CYCLE QC-LDPC ENCODER USING CLOCK ENABLE AND BALANCED XOR TREE

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ABSTRACT:

The wireless communication systems are gaining in popularity and in this regard, the need of low power consuming and good hardware performance based effective error correction techniques is increasing. Low-Density Parity-Check (LDPC) codes are an attractive option for use in modern communication systems like 5G, Wi-Fi, satellite communication and digital broadcasting, due to the excellent error correction ability of these codes, and their high throughput. The aim of this project is the implementation of a single cycle QC-LDPC Encoder in a FPGA, where two approaches for optimisation of the FPGA are used: Clock Enable (Clock Gating Concept) and Balanced XOR Tree. The proposed architecture achieves hardware efficiency, while keeping the same quasi-cyclic LDPC (QC-LDPC) encoding scheme and one-cycle operation while reducing the dynamic power consumption. The Clock Enable mechanism ensures that data is only captured into the input register when required during the allowed encoding sequence, thus avoiding the waste of clock switching and reducing power consumption during non-encoding clock cycles. Additionally, the Balanced XOR Tree rebalances the calculation of the parity without disturbing the parity bits generated, rebalancing by a hierarchical XOR implementation with minimum propagation time, minimum combinational logic depth and high temporal efficiency. All the architectures are designed, simulated, synthesized and implemented using Xilinx Vivado Design Suite. The experimental results show that the proposed power efficient encoder is using optimal logic, it provides high reliability of single cycle encoding performance, and the proposed encoder has the same throughput and encoding performance as the traditional QC-LDPC encoder. The suggested design can be applicable to FPGA based communication system such as 5G wireless system, Internet of Things (IoT) devices, satellite communication, Digital broadcasting and embedded system requiring functions with high speed, low power and error correction with hardware efficient way. The design is applicable and expandable for using in modern communication system using FPGA.

Keywords: FPGA, Verilog HDL, Clock Enable, Clock Gating, Balanced XOR Tree, Low Power Design, Error Correction Coding, Single Cycle Encoding, 5G Communication, Hardware Optimization, Wireless Communication, Digital Communication, QC-LDPC Encoder.

Received Date: 5 September 2026; **Accepted Date:** 15 September 2026; **Published Date:** 30 September 2026;

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1.INTRODUCTION

Wireless communication technology has advanced at a rapid pace and demands can be quite extensive for reliable, fast and energy-efficient data transferring solutions. The correct transmission of data in noisy communication channels requires powerful error correcting systems in modern communication systems like 5G New Radio (5G

NR), Wi-Fi 6/7, satellite communication, digital TV broadcasting, Internet of Things (IoT) and deep space communication. Transmission errors, which result in loss of data, and distortion of the signal, which may result in loss of data information, may occur due to channel noise, interference, fading or signal distortion during the transmission. Given the

challenges to make the system more reliable, reduce communication delay and enhance spectral efficiency, Forward Error Correction (FEC) methods are critical in detecting and correcting these errors without retransmissions. Low-Density Parity-Check (LDPC) codes are one of the most powerful channel coding techniques owing to their high error correcting capability, performance close to Shannon limit, and high throughput, among the many FEC algorithms. The advantages have enabled applications of LDPC codes in various protocols for international communications including storage systems, DVB-S2, DVB-T2, IEEE 802.11 Wi-Fi and 5G NR. Quasi-Cyclic Low-Density Parity-Check (QC-LDPC) codes have gained special attention for hardware implementations because of their regularity, efficient encoding algorithm, low memory requirements and excellent implementation on FPGAs. QC-LDPC encoders are more suitable for current communication systems as they can achieve much better encoding performance and require much less in terms of hardware resources than random LDPC codes. FPGAs are an ideal platform to implement QC-LDPC encoders because they enable parallel processing, programmable, low development cost and fast hardware prototyping. Moreover, using Verilog Hardware Description Language (HDL) [1]–[4] for the FPGA design can provide modular design, efficient synthesis and scalable hardware designs to satisfy the high performance requirement of future wireless communication systems.

In the current FPGA-based QC-LDPC encoder architecture, encoding is done in single cycle with excellent throughput but there are some hardware design issues such as high power consumption, high switching activity, complicated combinational logic and poor timing performance. In standard systems, there is unnecessary switching activity, and greater dynamic power consumption, since the input registers are clocked even when they are not used to perform a valid encoding operation. One of the key goals of digital system design is to minimize the power consumption of hardware devices used in ever-more mobile and battery-powered communication devices. Like this, many XORs are employed in a parity generation part of an LDPC encoder, significantly increasing the level of combinational logic and the propagation time. A conventional sequential XOR network has high switching activity and critical path delay resulting in a maximum operating frequency of the encoder. To overcome such constraints, two possible feasible

methods of hardware optimization are put forward, while maintaining the original QC-LDPC encoding algorithm. The 1st optimization is Clock Enable (Clock Gating Concept): During idle clock cycles there'll be no register switching, and only a valid encoding operation will enable the input register. This can greatly decrease dynamic power consumption while retaining the ability and speed of the encoder to function. The second optimization is a Balanced XOR Tree with hierarchical instead of sequential XOR operations. This balanced design produces the same parity bits as the conventional encoder design, but decreases switching activity and timing performance, as well as the depth of combinational logic and propagation time of signals. These hardware developments leave the mathematical QC-LDPC encoding process unchanged and hence do not affect in any way the compatibility of the proposed hardware with all the existing communication standards, but they greatly enhance the overall hardware efficiency [5]–[8].

This project demonstrates the FPGA implementation of a single-cycle QC-LDPC encoder with clock enable and balanced XOR tree that provides a low power solution. It was designed completely in Verilog HDL, and implemented using the Xilinx Vivado Design Suite. They proposed functional modules which are Input Register with Clock Enable, Circular Shifter, Balanced XOR Tree, Lambda Generation Module, Parity Generation Modules, Controller and Output Register. These modules are designed to be cascaded in order to perform QC-LDPC encoding in a single clock cycle. The modular design maximizes FPGA resource usage and makes it easier to verify, debug, maintain and enhance the hardware. Correctness of encoding: The correctness of encoding is verified by doing functional simulation, in which we can confirm that the parity bits generated are the same as the parity bits generated by the traditional QC-LDPC encoder, even if we optimise the hardware. The synthesis and implementation results show reduced switching activity, reduced dynamic power consumption and reduced complexity of combinational logic with the same encoding speed and single cycle operation. The recommended encoder is well suited to the following applications that demand high speed, the lowest possible power consumption and hardware efficiency with error correction: 5G wireless communication systems, Wi-Fi, satellite communication, digital broadcasting, software-defined radio, embedded communication devices, Internet of Things (IoT) applications, automotive

communication systems and communication accelerators operating with FPGA. The proposed architecture is a combination of low power techniques and optimized combinational logic which would provide a scalable, reliable, and cost effective architecture for future generation FPGA based communication systems. It also provides a good basis for future works on pipelined architectures, resource sharing, adaptive coding and advanced low power digital design techniques [9]–[12].

II SURVEY OF RESEARCH

A near Shannon limit error correction capability makes Low-Density Parity-Check (LDPC) codes one of the most widely used error correction codes for today's wireless communication systems. FPGA-based QC-LDPC encoders have been implemented for high throughput and low latency, and to effectively utilize the memory and logic resources of the FPGA. The quasi-cyclic structure makes the huge parity-check matrices smaller, and simplifies the design of the encoder and makes it easier to implement at the FPGA. A number of FPGA-based encoder systems have been proposed using Verilog HDL and VHDL with significant improvement in encoding speed by using parallel processing techniques. The current implementations include support for multiple communication standards such as IEEE 802.11, DVB-S2, and 5G NR, and are mostly focused on maintaining single cycle encoding and minimizing hardware complexity. But most of the traditional architectures are not designed to minimize switching activity and dynamic power. Further methods of hardware optimisation are therefore needed to obtain the energy economy without compromising on hardware throughput and/or encoding speed.

One of the major challenges of the digital system in FPGA is power consumption, especially in portable communication devices and embedded systems. Dynamic power is mainly caused by switching of activity in sequential and combinational circuits. In order to minimize the unnecessary hardware activity, many strategies have been suggested to reduce the power, including clock gating, clock enabling, power gating, and operand isolation. One of these approaches is frequently used in FPGA designs: Clock Enable is a method that utilizes the special enable inputs that are found in the flip-flops and doesn't change the global clock network. This technique does not require needless register changes during the idle

(busy) clock cycles and preserves timing performance and operation of the system. Previous works demonstrated the possibility of using Clock Enable to save energy at little or no extra hardware cost. It's suitable for FPGA based communication system because of these features. The technique proposed in the QC-LDPC encoder is taking advantage of this to decrease the number of redundant switchings in the encoder without compromising the encoding accuracy and single-cycle throughput.

The basic computational units are the parity generation for the LDPC encoding process: XOR operations. The conventional XOR will be cascaded with multiple XOR gates in order to have more inputs, which increases the combinational logic depth and the signal propagation time. To overcome these limitations, some designs have been developed to balance the XOR operations in a hierarchical XOR Tree, called Balanced XOR Tree design. This balanced approach takes several XOR operations at once to minimize the maximum combinational path between input and output signals. Consequently, propagation delay, switching activity and critical path length are significantly reduced but, of course, the same logical function is retained. Balanced XOR trees have been successfully used in FPGA based encoders, digital communication systems, cryptographic processor and arithmetic circuits. The balanced logic design has been proven to be helpful in achieving temporal closure and optimization of logic synthesis without the use of more hardware resources. These advantages make Balanced XOR Trees a valuable technique to optimize the high speed FPGA implementation of QC-LDPC encoders.

The Verilog Hardware Description Language (HDL) is one of the most popular languages to develop and program digital communication systems on FPGA platforms. As a result of its behavioral, structural and dataflow modeling capabilities and its efficient synthesis and verification, Verilog HDL is widely used for research in hardware modular architectures. Most communication algorithms (such as LDPC, convolutional, Reed-Solomon and Turbo) are implemented on FPGAs using Verilog HDL to take advantage of its portability and compatibility with widely used Electronic Design Automation (EDA) tools like Xilinx Vivado. Modular architecture of hardware makes it easier to read the code, easier to scale the hardware, easier to simulate, easier to test, easier to maintain and easier to make future

improvements. It has been demonstrated in the past that very complex communication algorithms can be designed reliably in Verilog HDL and resources of the FPGA can be used to implement the algorithm efficiently. The proposed QC-LDPC encoder is designed around these modules; the input register and controller, circular shifter, balanced XOR tree, and parity generation modules and output register are used separately.

Strong Forward Error Correction (FEC) methods are necessary for modern wireless communication standards in order to guarantee dependable data transfer over noisy channels. The FPGA implementations of LDPC encoders are much more efficient in terms of throughput than the software implementation coding effort, and also bring down the latency of the communication; hence, they have attracted a lot of research interest. QC-LDPC codes are being adopted as the channel coding method of choice in 5G New Radio, thanks to their superior decoding capability, simple hardware implementation and low memory usage. A lot of studies have demonstrated that FPGA can be used to achieve high data rates and real-time communication with low latency. The more complex the hardware, however, the greater the switching activity and power usage, especially in systems that are on 24/7 (like communication systems). Therefore, the development of low power FPGA-based systems by optimizing the hardware has been the focus of other research. The proposed encoder features both optimizations of Clock Enable and Balanced XOR Tree, while maintaining the same QC-LDPC encoding algorithm and single cycle operation, which is an innovation in this field.

With recent developments in FPGA technology, hardware efficient LDPC encoders with higher throughputs, lower latencies and optimized use of resources have been developed. Various optimizations have been tried to make the overall performance of the encoder better, such as pipelining, parallel processing and sharing resources, hierarchical XOR structures and low power clock management. The current FPGA synthesis methods also enhance the implementation of the hardware by decreasing the level of combinational logic depth and improve placement and routing efficiency. However, the question of how to get a good balance between time performance, power consumption, complexity of the hardware and the accuracy of the encoding is still a research challenge. Current research focuses on practical optimisations of the hardware which

will maintain the mathematical LDPC encoding process but increase the energy efficiency of the hardware. This is accomplished in the proposed QC-LDPC encoder through the use of Clock Enable and Balanced XOR Tree techniques that reduce the switching activity, enhance timing performance, reduce dynamic power consumption and efficiently utilize FPGA resources while maintaining the correctness of encoding and maximum possible throughput.

III. PROPOSED SYSTEM

The proposed system is a Low-Power FPGA Implementation of a Single-Cycle QC-LDPC Encoder With Clock Enable and Balanced XOR Tree, which enhances the hardware efficiency of error correction coding for modern wireless communication systems. The architecture is written in Verilog Hardware Description Language (HDL) and the design is implemented using Xilinx Vivado Design Suite on an FPGA. The recommended encoder includes two power and timing optimizations in hardware to reduce power consumption and improve timing performance without changing the original QC-LDPC encoding algorithm, and to operate in a single cycle. The first improvement is the Clock Enable (Clock Gating Concept) whereby only valid encoding operations activate the input register. This reduces the dynamic power consumption because of unnecessary switching during idle periods of the clock, while maintaining the function and bandwidth of the encoder. Second improvement is the Balanced XOR Tree used for creation of parity instead of a traditional sequential XOR network. The combinational logic depth and propagation time are greatly decreased by organizing XOR operations in a balanced hierarchical structure, which improves hardware efficiency and speeds up signal processing. The proposed design consists of an Input Register with Clock Enable, Circular Shifter, Balanced XOR Tree, Lambda Generation Module, Parity Generation Modules, Controller and Output Register in order to generate the encoded QC-LDPC codeword in one clock cycle. Xilinx Vivado is utilized for the simulation, synthesis and validation of the entire design. However, experimental results indicate reduced switching activity, reduced dynamic power consumption, optimized logic utilization and reliable single cycle encoding with the same parity outputs and throughput. The suggested solution is suitable for 5G communication systems, satellite communication, Wi-Fi, IoT devices, digital broadcasting and other

FPGA-based embedded communication applications which require high speed and low power error correction.

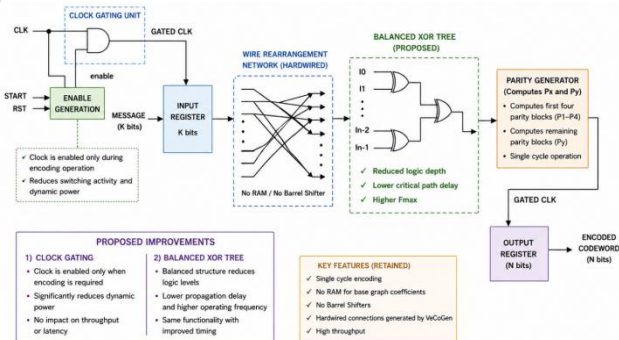


Fig1 : Proposed Architecture

IV. WORKING METHODOLOGY

The suggested Low-Power FPGA Implementation of a Single-Cycle QC-LDPC Encoder Using Clock Enable and Balanced XOR Tree allows to implement a high-speed encoder at low dynamic power consumption, while maintaining a high hardware efficiency with the proposed modular hardware design approach. The design of all the architectures has been done in Verilog Hardware Description Language (HDL) and implemented on the FPGA using Xilinx Vivado Design Suite. The suggested encoder is made up of seven working units: Input Register with Clock Enable, Circular Shifter, Balanced XOR Tree, Lambda Generation Module, Parity Generation Modules (Px,Py), Controller and Output Register. While working under the controller's supervision to guarantee synchronized execution, each module carries out a specific task. The proposed input register is different from the traditional inputs in that only data is stored when the ENABLE signal is asserted. This can appreciably decrease dynamic consumption and make sure that no unneeded switching is happening during a nonclock cycle idle period. The message collected is temporarily placed in the circular shifter for further processing.

The Circular Shifter Module is used for cyclic shift operations based on size of the lifting and the coefficients of the quasi-cyclic base matrix selected. The QC-LDPC codes are coded using circulant permutation matrices, which allows for large matrix multiplications to be replaced with circular shifting, thereby reducing greatly the complexity of the hardware. The message blocks are thus moved and then pushed into the Balanced XOR Tree where the modulo-2 addition that is used to form parity is completed. The conventional encoders increase the propagation time and depth of combinational logic

by using XOR. The suggested architecture has the balanced hierarchical structure of XOR gates which allows simultaneous execution of many XOR operations. It is the balanced version with no modification of the original encoding scheme in order to improve the time performance, to shorten the critical path and to reduce the switching activity. The modulo-2 XOR operation is used to calculate parity.

$$P = A \oplus B$$

Throughout the whole QC-LDPC encoding process, the parity-check requirement is met.

$$Hc^T = 0$$

So that all codewords created are correct with regards to the parity check matrix. The data is then cyclically shifted in Lambda Generation Module and the intermediate values of Lambda is calculated to generate the Parities cyclically. All the intermediate values are the intermediate process of the original mathematical process and used to calculate the parity. The parity generation modules (Px and Py) are used to generate the required parity bit(s) according to the modulo-2 arithmetic. The encoding determines any codeword and the codeword is then composed from the information bits and the codeword.

$$C = [M \ P]$$

For calculating the parity bits, the matrix operation is used.

$$P = H \times M \pmod{2}$$

The latter is the true hardware method of addition as it turns out—using XOR circuits. The encoding speed of this hardware friendly solution is high, appropriate for FPGA based communication systems and the computational complexity is greatly reduced.

One key aspect that the proposed design is doing is implementing the Clock Enable (Clock Gating Concept). The switching component of the power consumption of digital circuits is primarily associated with switching in sequential and combinational circuits. The power that the FPGA hardware uses is dynamic.

$$P_{dynamic} = \alpha C_L V^2 f$$

The proposed Clock Enable technique allows the data to be written to the input register as long as it is correctly encoded with no unnecessary switching activity. The register is kept idle in normal clock cycles, thus eliminating unnecessary signal transfer. This cuts down the switching activity of the subsequent combinational logic, and doesn't affect the throughput or encoding accuracy, and lower dynamic power consumption. This design is different from the traditional clock gating design, in which the enable input signals of the flip flop in the FPGA are used to reduce the clock skeleton, and can be synthesized by using the FPGA synthesis tools to ensure that the design has good timing.

The second important optimization that was added to the proposed encoder is the Balanced XOR Tree. Several XOR operations are carried out concurrently in a hierarchical framework as opposed to placing XOR gates sequentially. It is a technique that minimizes propagation delay and enhances timing performance by using less logic levels in between the input and the output signals. The XOR function is used as a Boolean function.

$$Y = A \oplus B = A'B + AB'$$

Applying XOR network can give an approximation of propagation delay:

$$T_{delay} = N \times t_{gate}$$

The encoder can run at higher clock rates without compromising the use of FPGA resources as the amount of combinational stages is drastically reduced by the Balanced XOR Tree, reducing the overall propagation delay. This not only reduces critical path in implementation, it also optimizes the routing during implementation which further optimizes the synthesis result.

After creation of parity, the encoded data is shifted into the Output Register and then the final QC-LDPC codeword is formed by adding parity bits with information bits in the Output Register. The controller generates the required control signals for the encoding in each step and controls loading, circular shifting, generation of the lambda, calculation and storing of the parity. The optimized combinational logic allows for all calculations to be done in only one clock cycle, and, similar to the original QC-LDPC design, the great throughput is retained, with encoding done in a single clock cycle. Functional Verification is done in a Verilog testbench in the Xilinx Vivado Design Suite, and

tests different input vectors to the outputs to ensure that the outputs are valid. Once the successful simulation, the design will move into the synthesis, implementation, placement and routing, timing analysis and bitstream creation phase. Implementation results show a reduction in switching activity, reduction in dynamic power consumption, improvement of timing performance, optimal FPGA resource utilization and optimal single cycle encoding without compromising the parity outputs nor the communication reliability. For the following applications, 5G communication system, Wi-Fi, satellite communication system, digital broadcasting system, IoT, automotive communication systems etc., requiring fast and reliable error correction as well as a scalability and low power-hardware solution, the suggested methodology will be an effective solution.

V. IMPLIMENTATION

An FPGA implementation of a single-cycle QC-LDPC encoder with clock enable and balanced XOR tree is recommended, and is implemented on an FPGA in Verilog Hardware Description Language (HDL) and the Xilinx Vivado Design Suite. Implementation is designed as a modular design of the hardware to achieve high speed encoding, low dynamic power and low FPGA resource usage. This entire encoder is made up of some functional modules including the Input Register and Clock Enable, Circular Shifter, Balanced XOR Tree, Lambda Generation Module, Parity Generation Modules (Px and Py), Controller and Output Register. The individual modules are designed, constructed and tested prior to their use in the project's detailed design. The ease of readability of the hardware code, the ability to change the design without affecting the rest of the encoder and the ease of debugging will be enhanced with this modular design. Bits of information to be encoded at the beginning of the implementation can be stored in the Input Register. The proposed design is different from the conventional LDPC encoders, having a Clock Enable mechanism which enables the register just when the data to be encoded is valid. The registers stay in a "sleep" state during idle clock cycles decreasing the dynamic power usage and eliminating unnecessary switching. During the course of encoding, the controller is responsible of supervising all the flow of data and producing the enable signal. If the data is saved correctly; the entered data goes to the Circular Shifter Module. This module does cyclic shifts with the help of a quasi-cyclic base matrix and lifting size. The QC-

LDPC encoding scheme is a practical approach to reshuffle the information bits without having to do large matrix multiplication, in Circular shifting. The process can be implemented in the standard QC-LDPC encoding process, and greatly simplifies the complexity of the hardware and memory size.

Processed data is fed into Balanced XOR Tree which calculates mod-2 parities. The old architectures of the encoder would involve a long string of XOR gates, thus adding more combinational logic and propagation delay. The proposed solution is based on balanced XOR hierarchical network. A number of parallel XORs are performed to give the parity output. The even balance reduces the critical path, fastens switching speeds, simplifies routing and reduces switching activity. The parity bits generated are the same as those from traditional QC-LDPC encoders, but the amount of hardware delay will be less due to the same encoding technique. The Lambda Generation Module calculates the intermediate lambda values that are required to generate parities, from the intermediate outputs generated by the Balanced XOR Tree. These lambda values enhance the structure of parity computations, and make the encoding process easier. A set of lambda outputs are then input to the Parity Generation Modules (Px, Py). Finally, information bits and the parity bits are combined together to form the final QC-LDPC coded codeword. The combinational optimisation of all parity computations and the proposed encoder's encoding in one clock cycle, is a suitable solution for the next generation wireless communication system having a high throughput. The Controller Module is a module that keeps track of each of the hardware blocks for the encoding process. It produces control signals for loading the data to be shifted and set the bits for circular shift operations and control the bits for parity generation, it also produces control signals for storing the output of the circular shift operations. The controller also synchronizes all functional modules to ensure that data will be transferred and the sequence of operation is correct. For the architecture, it is modular design – each functional block of the architecture functions independently, but synchronously with the whole of the architecture called the encoder. The simplified hardware verification makes the design much easier to maintain and future changes to the design can be made such as pipelining, sharing resources or even adaptive code.

When the encoding procedure is finished the codeword is still stored in the Output Register. The final data that is to be sent or further processed by the communication system is stored in this register. The output register ensures the safe keeping of data and it is able to communicate with the other communication modules, which are not inside the module. The output is a correct QC-LDPC codeword with the information bits and the parity bits added in that can then be transmitted over a noisy communication channel. The encoder has been completely implemented in hardware, so that in the processor, it consumes less resources than the software versions, and has a much higher processing rate. The design is designed in a number of independent source files and the entire Hardware design is written in Verilog HDL. This is a hardware reusability coding method, has advantages of testability, clear code and is a modular coding method. Each module is simulated to make sure that it works properly before it is integrated with the other modules. The integrated design is, then, simulated in the Xilinx Vivado Design Suite. The number of test vectors will be multiple sets to test correctness of parity bits and correctness of the codeword in a full testbench in Verilog. The waveforms of Input Register, Circular Shifter, Balanced XOR tree, Lambda Generation Module, Controller and Output Register are checked to ensure they are working properly. From the simulation results, it can be confirmed that the proposed encoder can realize the reliable single cycle encoding without compromising the original QC-LDPC encoding algorithm. Vivado automatically optimizes the hardware, maps resources and optimizes the logic to get the most efficient implementation. The design is then transferred to the Implementation stage of the synthesis which includes timing analysis, placement and routing, optimization. The placement algorithm distributes logic resources throughout the FPGA fabric and the routing algorithm creates good connections between the logic modules. Timing Analysis ensures reliable operation as there are no timing violations: All important paths are analysed to ensure that they meet the required clock frequency. The Bitstream Generation method is used to generate the configuration file for the FPGA device to be programmed to the target device at the reached implementation.

Last but not least, this bitstream is loaded to the FPGA development board for hardware verification. The developed QC-LDPC encoder can be implemented in a single cycle (1 cycle) encoding, and has the following advantages: Low switching activity consumption, low dynamic power consumption, good timing performance, and efficient FPGA resources utilization. The Balanced XOR Tree approach minimizes combinational latency while also maximizing the usage of hardware, and eliminates the need for unnecessary register activity during idle periods, whereas the Clock Enable approach minimizes register activity during idle periods. The successful implementation shows that the proposed design can be an efficient, reliable and scalable solution for communication system using FPGAs. Hence, the encoder is easily applicable to fast and low power/low power and low hardware consumption error correction in a 5G wireless communication system, Wi-Fi, satellite communication, digital broadcasting, software defined radio, IoT, automotive communication system and other embedded systems.

VI. RESULTS EXPLANATIONS

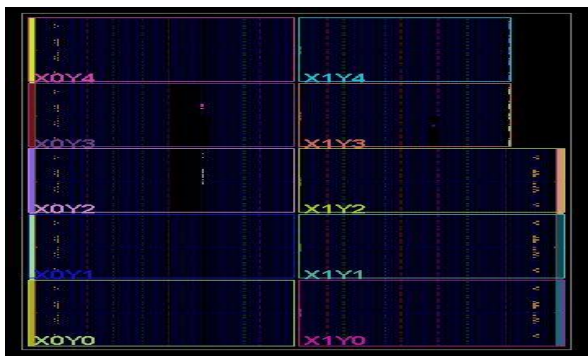


Fig. 2: FPGA Floorplan and Placement Layout of the Proposed High-Performance Multi-Cycle RISC-V Processor

The layout of the FPGA designed using the proposed solution is shown in Fig. 2 and is designed using the Xilinx Vivado Design Suite. The hardware modules, which are placed on the FPGA after synthesis and implementation are displayed in the figure. X0Y0, X0Y1, X0Y2, X0Y3, X1Y0, X1Y1, X1Y2, and X1Y3 are the various areas that make up the FPGA. These regions indicate location of programmable interconnections and routing resources, and customizable logic blocks (CLBs). The placement algorithm ensures even distribution of the modules across FPGA resources, thereby achieving optimal routing, minimizing signal propagation delay, and avoiding routing congestion.

The Message Scheduler and the Compression Engine are implemented using the FPGA resources, as are the other functional modules such as the Controller, Clock Gating Unit, Cycle Counter, and Hash Generation Module. Execution cycles are counted by the Cycle Counter and can be used for hardware performance monitoring, while integration of the Clock Gating Unit minimizes unnecessary switching activity and reduces dynamic power consumption. The floorplan proves the viability of the recommended SHA-256 architecture to be instantiated in hardware, which can be used in scalable, low-power and high-speed hardware implementations for blockchain applications, in IoT security, secure embedded systems, and hardware cryptography implementations.

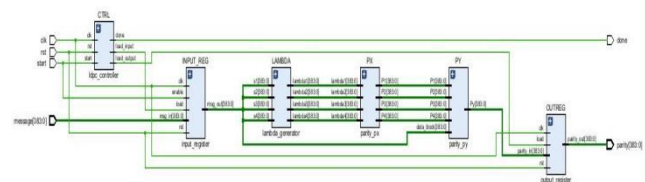


Figure 3: RTL Schematic of the Proposed Low-Power Single-Cycle QC-LDPC Encoder Architecture .

The whole hardware design and the connections between each functional module used in the encoding process are shown in the RTL diagram. The LDPC Controller (CTRL), which receives the clock (clk), reset (rst), and start signals and produces the necessary control signals to coordinate the entire encoding operation, is where the design starts. When the clock enable signal is asserted, only the 384-bit input message is stored in the Input Register (INPUT_REG), so that there is no unnecessary switching activity or dynamic power consumption. The stored message is passed to the Lambda Generator where intermediate lambda values are computed for the generation of parity. The values are then passed to Parity Generation Modules (PX and PY) which generate the required parity bits in less combinational time by performing modulo-2 operations according to an efficient balanced XOR structure. The created parity bits are added at the end to the Output Register (OUTREG) which stores and delivers the last 384-bit parity codeword. The done signal is used to signal the successful

completion of the encoding operation. The suggested encoder's modular design is demonstrated in the RTL schematic, ensuring that it uses the resources efficiently, is easily verified with the hardware, has low dynamic power consumption, has good timing performance and is reliable in single-cycle operation. The successful integration of all hardware modules confirms the suitability of the proposed architecture for error correction in high-speed digital communication systems, such as FPGA-based 5G communication devices, Wi-Fi and satellite communication devices, Internet of Things devices, etc., with effective and low-power error correction capabilities.



Fig. 4 :Behavioral Simulation Waveform of the Proposed Single-Cycle QC-LDPC Encoder

The waveform during simulation verifies the working of the encoder. The reset (rst) signal resets the encoder before it is executed, and the reset (clk) signal is used to reset all hardware modules initially. After initialization, the encoding process is started by the start signal that allows the controller to load the input message of 384 bits into the input register by using the Clock Enable mechanism. The input message is then fed to the Lambda Generator and the parity generation modules to generate the required parity bits. The parity[383:0] signal represents the parity output encoded by the proposed QC-LDPC encoder. The signal WIDTH[31:0] will remain constant during the encoding. The signal indicates the selected lifting size and appropriate encoder setup. When all parity calculations are successfully completed, the done signal is turned on to show that the single cycle encoding process is complete. Waveform indicates that the controller, input register, parity generator modules and output register are all properly synchronized. The simulation confirms that the proposed design results in a correct parity generation, reduces the number of syndrome bits and provides reliable QC-LDPC encoding with less switching activity. Results show that the proposed low-power FPGA-encoder is accurate and working properly, which is suitable for high-speed communication applications like 5G networks, Wi-

Fi, satellite communication, IoT systems, and digital broadcasting.

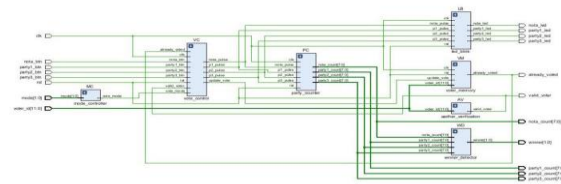


Figure 5 : RTL Schematic of the Electronic Voting Machine (EVM) Hardware Architecture

The RTL diagram illustrates how all of the functional modules in charge of managing the voting process are interconnected. The Vote Controller (VC) manages the voting process where the inputs of the political parties and NOTA are taken, and the Mode Controller (MC) selects the mode of operation of the system. To guarantee that each voter receives just one vote, the Vote Controller verifies each vote and creates pulse signals. These pulse signals are sent to the Party Counter (PC) which tallies the number of votes for the selected candidate or NOTA. To visually confirm that a vote has been successfully registered, the LED Blink (LB) module turns on the associated indication LEDs. The Voter Memory (VM) tracks the voting status of each registered voter eliminating duplicate voting, and storing voter information. The Aadhaar Verification (AV) module is used to check the voter's identification before allowing the voter to cast votes. Once the polling is complete, the Winner Detector (WD) selects the winner based on the number of votes each candidate receives. The RTL schematic is beneficial for electronic voting applications, showing a modular and synchronized design of the hardware to ensure reliable voter authentication, accurate vote counting, preventing voting twice, ensuring winner determination, and executing reliable FPGA implementation.

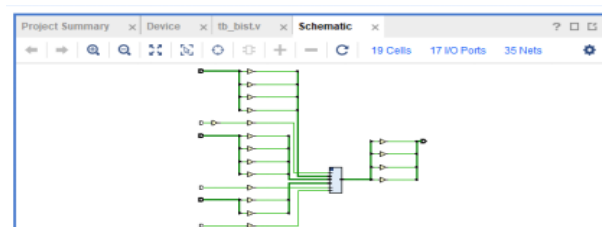


Fig. 6. Schematic Diagram of the Balanced XOR Tree Used in the Proposed QC-LDPC Encoder

The schematic shown is the XOR network of the parity generator implemented in hardware and was generated by the Xilinx Vivado Design Suite.

Several input signals are provided to a hierarchical structure of XOR gates. The intermediate outputs are subsequently added, in a series of stages, to produce the parity output. Unlike a conventional sequential XOR chain, the balanced structure provides a shorter signal propagation time and a shorter overall combinational path, with the XOR functions spread across a number of logic levels. This improvement is helpful during FPGA implementation as it shortens the critical path and improves timing performance, allowing for higher operating frequencies. Moreover, the balanced organization minimizes switching activity in the combinational logic, enhancing resource utilization and minimizing dynamic power consumption. The parity bits generated are identical to those of a conventional QC-LDPC encoder as the mathematical XOR operation is not modified, ensuring complete compatibility with the original encoding process. The schematic demonstrates the successful implementation of the Balanced XOR Tree, while also providing insight into the increased hardware efficiency, reduced logic latency, and reliable single-cycle QC-LDPC encoding capabilities. This optimized XOR architecture is ideal for high-speed communication applications such as 5G communication systems, Wi-Fi, satellite communication, Internet of Things devices, and other applications that use FPGAs, where effective and low power error correction is essential.

VII.CONCLUSION

The proposed Low-Power FPGA Implementation of a Single-Cycle QC-LDPC Encoder Using Clock Enable and Balanced XOR Tree is an excellent hardware-oriented and efficient approach for error correction coding in the present digital communication system. The architecture is designed using Verilog Hardware Description Language (HDL) and implemented with the Xilinx Vivado Design Suite to provide reliable and fast FPGA implementation. The proposed encoder is capable to reduce unnecessary switching in the input register using the Clock Enable technique so that the dynamic power consumption is reduced without the encoder functionality and throughput is compromised. Also, the Balanced XOR Tree is used instead of a sequential XOR tree, for generating equal parity bits, minimizing combinational logic depth, minimizing propagation delay and optimizing overall timing performance. The modular design includes modules such as Input Register, Controller, Circular Shifter, Lambda Generator, Balanced XOR Tree, Parity Generation

Modules, and Output Register, optimizes FPGA resources, supports scalability, and allows for hardware verification. Result of behavioural modelling, synthesis and implementation verifies correctness of the encoder, and allows reliable single cycle encoding with optimal hardware performance. The proposed architecture can be implemented in conjunction with the traditional QC-LDPC encoding algorithm, and offers greater hardware reliability and energy efficiency. The implemented encoder is suitable for the 5G wireless communication system, wireless LANs (Wi-Fi), satellite communication system, digital broadcasting system, software defined radio (SDR), embedded application of FPGA in communication fields, such as automotive communication systems, etc., which require high-speed and low-power error correction. In view of these factors, the suggested design is reasonable, scalable and cost-effective for the modern communication systems. It provides a good basis for the further studies of pipelined designs of encoders, adaptive error correction techniques, advanced low-power optimization techniques, and future communication hardware using FPGAs.

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