

AI-DRIVEN RTL GENERATION WITH ADAPTIVE ERROR CLASSIFICATION AND FUNCTIONAL VERIFICATION

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ABSTRACT:

With the complexity of today's digital systems, the demand for advanced Electronic Design Automation (EDA) tools that can accelerate the design of hardware and ensure its functionality has increased. In traditional Register Transfer Level (RTL) design, engineers have to write design specifications in Verilog Hardware Description Language (HDL), a process that is tedious and prone to errors, and requires extensive verification and debugging. This project proposes an innovative approach to creating Verilog HDL automatically by using a Large Language Model (LLM) and an adaptive error categorization and verification process, called IntelliRTL. The proposed system automatically generates synthesizable Verilog HDL code when accepting natural language (NL) design specifications. Unlike standard RTL generation system, IntelliRTL has an Adaptive Error Classification Module that categorizes the code generation error into logical, syntax and compilation error before functional verification. The system keeps unnecessary debugging cycles and increases the effectiveness of the verification process by giving specific feedback depending on the problem category found to enhance output HDL. The RTL is automatically tested for functionality and simulated with tools before FPGA implementation. Iterative feedback greatly improves code dependability, speeds up development, and raises the likelihood of producing accurate hardware designs with little assistance from humans. The proposed framework includes support for rapid prototyping, FPGA/ASIC development, digital system education, and automated design with the help of AI. With its intelligent code generation, adaptive error analysis and automated verification, IntelliRTL provides an effective, scalable, and reliable solution for next-generation RTL design workflows. This improves the quality of hardware design, reduces complexity, and increases the productivity of hardware design in modern semiconductor technology.

Keywords: Register Transfer Level (RTL), Verilog HDL, Large Language Models (LLMs), Automated RTL Generation, Adaptive Error Classification, Functional Verification, FPGA, ASIC, Hardware Design Automation, Artificial Intelligence (AI), and Electronic Design Automation (EDA).

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I. INTRODUCTION

With rapid advances in semiconductor technology, modern digital systems are a lot more complex and sophisticated, increasing the demand for efficient and ingenious techniques for the design of hardware. For today's application such as embedded controllers, Internet of Things (IoT) devices, automotive electronics, communication systems and Artificial Intelligence (AI) accelerators, a high

reliability, short design cycle digital circuits are needed. The traditional way to design a register transfer level (RTL) is to model, debug, synthesize and verify the design after manually translating the hardware specifications into hardware description language (HDL) code, such as Verilog or VHDL. While it works to get reliable hardware implementations, this approach is very cumbersome, needs hardware engineer expertise, and can also generate logical errors, syntactical errors and

compilation errors leading to a high design and hardware validation cost. Recent developments in artificial intelligence (AI), especially Large Language Models (LLMs), have shown impressive skills to comprehend natural language and produce source code, creating new possibilities for automating the creation of hardware descriptions. Embedding AI in Electronic Design Automation (EDA) software can help designers cut down repetitive coding tasks, boost productivity, and accelerate RTL development. Therefore, the problem of intelligent RTL generation has been a viable field of study to enhance the efficiency of the hardware design process in general, and of the FPGA and ASIC design processes in particular [1] – [4].

Combining the power of LLM and adaptive error classification and verification mechanism, IntelliRTL is a hybrid approach that offers an intelligent framework for automatic Verilog HDL production. The proposed structure also features an Adaptive Error Classification Module that can detect syntax/ compilation and logic errors before the verification phase, which is an advantage over the traditional HDL code generating systems that pass generated code to the simulation phase. This additional module can be useful to the framework for reducing unnecessary debugging cycles and enhance output RTL quality by using repair techniques specific to the fault observed. The generated Verilog module is automatically compiled, functionally simulated and verified by testbench and then programmed into FPGA. The iterative process of feedback creates more and more code until you get the desired functionality and so enhances reliability and reduces development time. The proposed design would have less human interference in the code generation process, and by using intelligent code generation and automatic verification, synthesizable and function correct HDL will be generated. This would be helpful in the modern semiconductor technology to help in rapid prototyping of industrial and educational devices, improve productivity and reduce the development cycle of the hardware devices [5]–[8].

As more companies begin using AI-enabled Electronic Design Automation, engineers can now concentrate on solving new and challenging design problems, rather than being inundated with the drudgery that is

implementation. The IntelliRTL framework helps further this development by integrating smart code generation, adaptive error analysis and verification-based refinement in a single development process for a hardware device. The proposed solution not only allows the improvement of functional correctness, but also creates scalable and maintainable RTL code, which can be used to design embedded systems, to design FPGA prototypes, to design ASICs, in communicating hardware and for educational research. Furthermore, the framework offers a flexible architecture for expansion with additional features like multi-agent cooperation, timing analysis, resource optimization, power estimation and the integration of other hardware description languages like SystemVerilog and VHDL. Intelligent HDL (HDL) generating framework will be one of the most important components of the next generation of EDA tools that will greatly simplify design complexity and speed the semiconductor product development process as AI continues to progress. Thus, IntelliRTL is a viable and scalable approach for intelligent hardware design automation, which can support the future development of digital systems, improve engineering productivity, improve design quality and increase verification efficiency [9] – [12].

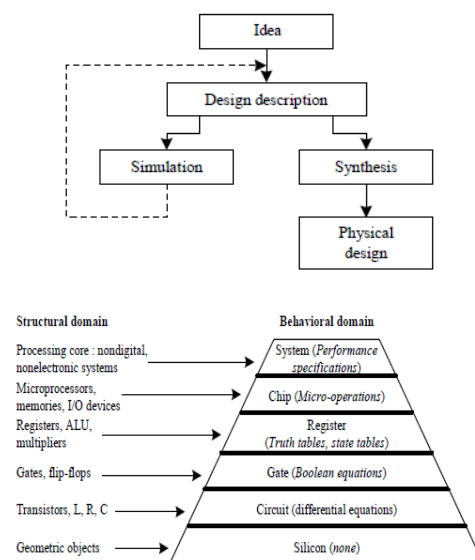


Fig1 : Asic Design Flow

II SURVEY OF RESEARCH

The Electronic Design Automation (EDA) technology has revolutionized the creation of

digital hardware systems, with an automated approach to design, synthesis, simulation and verification. The Register Transfer Level (RTL) design was manually coded previously using either of the Hardware Description Languages (HDLs) used which included Verilog and VHDL and required a high level of engineering knowledge and a lot of development time. With increasingly complex semiconductor devices, faster design cycles and higher productivity and reliability are necessary, characteristics which were difficult to achieve using traditional design methods. To facilitate the automatic hardware development procedure, researchers have been exploring Artificial Intelligence (AI) solutions. With recent advances in Large Language Models (LLMs), the ability of these models to understand natural language and generate code has demonstrated its impressive programming capabilities, which is the reason for researchers to extend these capabilities to automatic HDL generation. The developments have offered an excellent basis for intelligent generation of RTLs that can improve the efficiency of hardware design and the quality of hardware verification with lower coding efforts [1]–[3].

There have been several experiments that have directly synthesized Verilog HDL from natural language specifications with a LLM. Thanks to these ingenious technologies, designers can even describe hardware functionality using text which allows the AI models to generate equivalent RTL implementations. Experimental tests have demonstrated good performance in the design of arithmetic circuits, finite state machines, counters, multiplexers and communication interfaces. However, academics have discovered several limitations like wrong sequential logic implementation, wrong assignment of signals, wrong module declaration, syntax error and functional error. Even in the case of hardware development using AI-generated HDL, validation is an important process in the development process because generated HDL codes must be validated before use. Combining these

automated-verification techniques with HDL production has been the focus of current research efforts, not only for functional accuracy but also to decrease the human debugging effort and to increase verification confidence in the generated RTL implementation before deployment into FPGAs or ASICs.

The study of verification in today's semiconductor design is important because they make sure that the hardware has the correct functionality and time before it is actually used. There are several existing verification methods, for example, simulation-based, assertion-based, constrained-random, formal verification, and coverage-driven verification. Automated testbench generation has a huge positive impact on verifying different operational scenarios without having to invest a lot of work into the task. A set of test scenarios are provided and the simulation tools are run using the modules created from RTL, the results are compared with the expected functional behavior. Although these techniques are effective for detecting hardware errors they generally only begin to detect errors after simulation has begun, and if they miss any syntax, compiler or logical errors, debugging cycles are repeated again. This limitation not only makes verification more time-consuming, but also makes the design of the hardware more complicated. This is why researchers are motivated to investigate clever techniques of verifying the hardware in order to detect and categorize faults in the hardware design at an early stage of development [7]–[9].

In recent years, with the development of AI technology, the ability to process compiler reports, synthesis logs, and simulation results to draw conclusions about the root cause of hardware design errors has been brought about by intelligent debugging tools. Using machine learning algorithms and AI supported reasoning systems, HDL faults are categorized as grammar, compilation, time and logical class and suitable corrections are proposed. These

method can greatly lower the level of debugging complexity by offering specific feedback as opposed to regular manual checks. Moreover, intelligent error analysis reduces and accelerates the verification process by enabling developers to fix any important errors before running tedious simulation processes. But most of the existing systems only classify the error only after the verification process starts, limiting its ability to lower the number of unnecessary iterations of the verification process. Attempts are still being made to increase the overall design productivity and functional correctness of the overall hardware design by directly mapping the adaptive error analysis methods for automatic RTL generation [10]–[12].

Conceived recently, agent-based artificial intelligence (AI) is a potential architecture for solving difficult engineering problems by distributing the development effort among multiple agent-based specialised developers, who will collaborate during the design process. Agent-based RTL generation frameworks automatically analyse specifications, synthesize HDL code, verify, debug and refine it in digital hardware in an iterative manner, and feed each other with constant feedback and communication. Modular architectures give scalability, maintainability and flexibility as each functional module can be improved individually and without impact to the overall architecture. Iterative refinement greatly enhances the accuracy and quality of generated RTL code, according to earlier studies. But, there are yet no facilities in these existing agent-based systems to classify the errors before verification, so it is possible that the error is a syntax or compilation error, in which case the agent would have to simulate and debug that error repeatedly. This is still an ongoing challenge in the field of AI aiding Electronic Design Automation [13]–[15].

Artificial Intelligence, Large Language Models, automated verification, and intelligent debugging, as clearly demonstrated in the

literature, are a huge leap forward in the modern approaches to hardware development. There are however some points that require further improvement, including several verification cycles, not so effective debugging and using adaptive error analysis in RTL development. In order to get around these restrictions, the suggested IntelliRTL architecture includes an Adaptive Error Classification Module that finds logical, syntax, and compilation issues prior to functional verification. The advantages of this improvement are enhanced reliability of automatically generated Verilog HDL, reduced need for unnecessary verification iterations and the ability to take corrective action on a specific basis. The proposed solution combines the features of AI-assisted code generation, adaptive error classification, automatic code verification, and automatic error refinement into a single architecture for scalable, intelligent and effective RTL generation for FPGA prototyping, ASIC development, embedded systems and the next generation Electronic Design Automation world [16]–[18].

III. WORKING METHODOLOGY

It's one electronic design automation (EDA) framework that combines automated verification, adaptive error categorization, large language models (LLMs), and iterative refinement. The user provides a specification for the digital circuit, i.e. a specification of the required functionality. The specification is pre-processed and then encoded as a structured prompt before being fed to LLM to generate RTL. The specification is preprocessed and converted to a structured prompt before it is fed to the LLM to generate the RTL. An Adaptive Error Classification Module is used to identify syntax, compilation and logic errors in the resulting HDL prior to functional verification. This is the pre-processing phase that enhances the quality of the generated RTL and skip out un-necessary simulation cycles. This optimized HDL is then automatically tested using automated testbenches, the results of the simulation are presented as code, which can be synthesized to an FPGA or ASIC, to verify all the functional requirements. This enhanced HDL is then simulated using the automatic

testbenches to satisfy all the functional requirements, and testbench output is converted to the required FPGA/ASIC code.

Let's take a look at the following model for the hardware specification:

$$S = \{s_1, s_2, \dots, s_n\}$$

The functional requirements are shown by the "where (s_i)" and Design specification is shown by the "where (S)". The Large Language Model is used to convert the specification to RTL code.

$$H = f_{LLM}(S)$$

where (f_{LLM}) represents the language model which translates plain language specifications to synthesizable hardware description (H) is Verilog HDL. This automatic translation also can greatly save the manpower of manual coding, while keeping consistency of the hardware modules. The HDL produced according to the requirements contains Module Declarations, Input-Output Ports, Combination logic and Sequential logic, Arithmetic operations and descriptions of Finite State Machines. Many factors come into play for the output RTL quality; the following reasons are of particular interest: the clarity of the input specification, the reasoning ability of the language model. Among these, the clarity of the input specification and the reasoning ability of the language model are of particular interest [4]–[6].

Proposed Solution Design: Post HDL synthesis Adaptive Error Classification Module (AECM) looks at the synthesized Verilog code prior to functional Verification. This module determines the sort of error and sends the necessary feedback to the refinement engine, in contrast to conventional RTL generating systems that go straight to simulation. Is classified under:

$$E = \{E_s, E_c, E_l\}$$

where (E_s) represents the number of syntax errors, (E_c) is the number of compilation errors, and (E_l) is the number of logical errors. The rule for identifying rows of the data.

$$C(H) = \arg \max P(E_i|H)$$

The most likely errors of the generated HDL ($C(H)$) are indicated by the category. The overall development efficiency is also increased and the complexity of verifying the lower one can be realized by the classification

of the errors in the early stage of development[7]–[9].

Once the faults are corrected, the HDL code is automatically compiled and tested using pre-defined testbenches. The verification module compares the outputs of the design specification to the simulated outputs. Consider, $y_{\text{simulated}} = (Y_p)$ and $y_{\text{expected}} = (Y_e)$. The functional accuracy is checked using:

$$A = \frac{N_c}{N_t} \times 100$$

Where N_t is the number of test cases that have been run and N_c is the number of test cases that have been passed. If the verification accuracy is near 100%, then the resulting RTL will be able to comply with all the functional requirements. If it does not match, then it goes through another refinement until it reaches full functional correctness – continuously improving the HDL until it is correct [10]–[12]. Adding the verification feedback at later stages of HDL creation leads to continuous improvement of the RTL, through iterative refinement. The refining process can be mathematically represented as

$$H_{i+1} = H_i + \Delta H$$

where (ΔH) are the corrections applied with the classified errors and verification feedback, (H_i) is the current RTL implementation. Until the process is repeated until the initial shape turns into the target shape.

$$Error(H) = 0$$

Being able to show that there are no logical, syntactic or compilation problems in the generated HDL. Compared with the traditional RTL development approaches [13]–[15] this feedback system is more efficient to enhance the reliability of the hardware and to decrease the debugging process. The proposed framework is evaluated in terms of functional correctness, error reduction rate and efficiency of verification. The percentage reduction of mistakes is calculated as

$$ER = \frac{E_b - E_a}{E_b} \times 100$$

Before adaptive correction errors (E_a) and adaptive correction errors (E_b). The higher the (ER) value, the more effective Adaptive Error Classification Module will be. Another measure to quantify the efficiency of verification is the number of verification

iterations that are required to generate functionally correct RTL. Experimental evaluation [16]–[17] has demonstrated that at this early stage of error categorization, the simulation cycles required to synthesize the hardware are reduced, the hardware is synthesized of higher quality, and overall hardware development time is decreased. Finally, the validated Verilog HDL is synthesized using FPGA design tools like Xilinx Vivado or Intel Quartus to assure the hardware compatibility and implementation. The resulting RTL is synthetically correct, synthetically viable and can be implemented in the FPGA or ASIC platform, if it can be synthesized. Intelligent code generation, adaptive error analysis, automated verification, and iterative refinement are all combined in the suggested IntelliRTL framework to provide a scalable hardware development process that can lower design complexity and boost engineering productivity. The modular design and the support of new timing analysis, resource optimization, power estimation, and SystemVerilog and VHDL make it suitable for next generation AI-enabled Electronic Design Automation environments [19]–[22].

IV RESULTS EXPLANATIONS

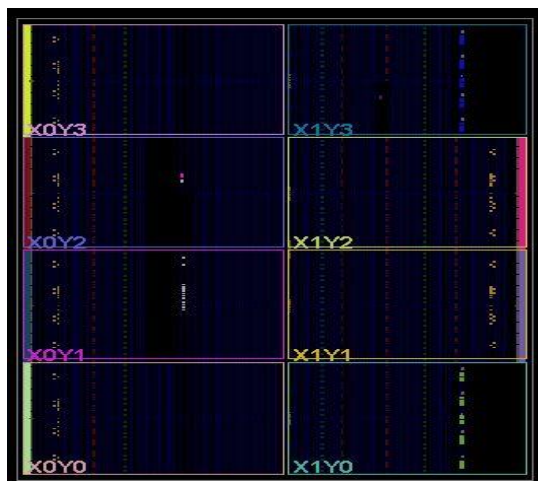


Fig. 2: Synthesis Results

The synthesized Verilog HDL code was synthesized using FPGA synthesis tool and the post-synthesis implementation results of the proposed IntelliRTL framework are presented

in Fig. 2. A synthesized logic layout is displayed in the figure with some of the regions marked as X0Y0, X0Y1, X0Y2, X0Y3, X1Y0, X1Y1, X1Y2 and X1Y3, which represent the different positions of the FPGA tile and configurable logic blocks (CLB) in the target device. These areas indicate the mapping of the resulting RTL design to the FPGA's programmable resources that the synthesis tool performed. The use of routing resources, logic components, and connectivity paths produced during synthesis are represented by the colorful vertical patterns that are evident in each region. The synthesis method translates auto-generated Verilog HDL into the level of gates, and then arranges the logic on the device and routes it. Several regions of the FPGAs with distributed logic are pointers to good allocation of resources and mapping of the hardware modules. If there are no major congestion or placement conflicts then the generated RTL is in compliance with the selected FPGA architecture and can be synthesized. Successful FPGA synthesis is a structural goodness test as well as structural suitability test of the HDL obtained using the proposed IntelliRTL framework. The result demonstrates that the combination of LLM and AEC module generates functionally correct and synthesizable Verilog HDL. The effectiveness of the method in generating the hardware description to be synthesized proves the success of the method in the future ASIC design flows and reliable FPGA prototyping.

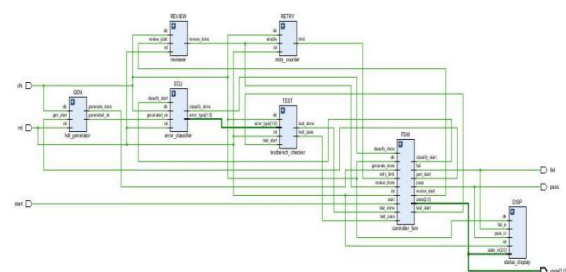


Fig. 3 Proposed IntelliRTL Architecture

Fig. 3 shows all the hardware architecture of the proposed IntelliRTL

framework which generates automatically functionally correct RTL code from Verilog HDL generation, error classification, verification and iterative refinement. An architecture is comprised of a number of functional modules that are interconnected and deliver control and status communications. The process is triggered by the input signal called 'start' and the whole workflow is executed synchronously with a common clock signal 'clk' and reset signal 'rst'. The HDL Generator (GEN) module is used as the first module for the architecture. It automatically generates the Verilog HDL program, once it receives the clock, reset and generation start signals, based on the given hardware specification. Once the HDL is created, it can be used for further testing, since the module will set the generate_done signal as the RTL code is generated. The key enhancement added to the proposed IntelliRTL framework was the Error Classification Unit (ECU) to which the generated HDL was then sent. This module takes as its input output a resultant Verilog code and categorizes all the faults into different categories such as syntax error, compilation error, logical error etc. The signal 'error_type' is used to pass the classification result and the signal 'classify_done' is used to indicate that the classification is completed. Being able to identify the type of error in early stages, enables targeted repair and minimizes the number of iterations to verify for errors. Once the error is correctly classified it is passed to the next module, the RTL code verifier, TEST. This block is used to run predefined test cases for automated functional testing using the HDL created. The results obtained from the simulation are compared to the expected results to check whether the design is working. The module provides the controller with the feedback from the verification (pass, fail, test_done signal).

If verification is unsuccessful the Retry Counter (RETRY) module is triggered. This

module stores a count of how many times it is retried on the refinement process and ensures that repeated verification processes are carried out until an RTL is generated which satisfies all functional requirements and/or until the retry limit is reached. This is an iterative refinement process that can produce more functional and synthesizable HDL without entering into an endless loop of iterations. The Finite State Machine (FSM) controller will be responsible for the overall operation of the system. The FSM provides control over the various components of the HDL synthesis, error classification, verification, retries handling and final result generation. Based on the status signals received from each module, the controller decides the next execution state and also makes sure that the workflow is executed in the right order. This centralized control assures reliable functioning of the whole structure and synchronization. Lastly, the final execution status will be displayed on the module Display (DISP) and the modules Log Design (LOG) and Log Verification (LOG) will write the created design/verification information to a log for analysis. The design includes output signals to indicate the current state of the controller and whether the HDL code is validated to perform the correct function including pass, fail and state[2:0]. The proposed architecture of IntelliRTL is designed to present intelligent HDL generation, adaptive error classification, automated testbench verification, automatic retries, centralized control, and integrate them into a single-flow chain for effective, reliable and scalable RTL generation which can be used for FPGA and ASIC design automation flow.

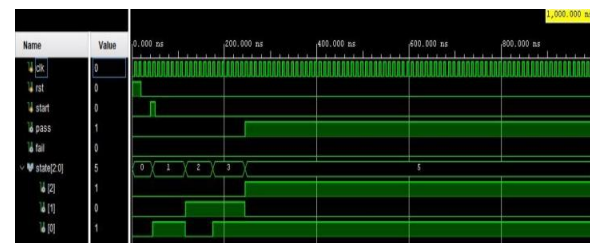


Fig. 4 Simulation Results

The time correlation of the input control signals, the internal state transitions and the output status signals during the operation process is displayed in the waveform, thus proving the correctness of the operation of the system. The simulation time-range for the simulation is: 0ns to 1000ns and the sequential flow of RTL generation and verification is shown. The reset signal is one that resets the hardware to the known state at the beginning of the simulation and the clock is a steady signal that may be used to synchronize all the hardware modules. Proposed structure is activated using the signal, start, which starts HDL synthesis and then the verification process. As the controller processes the FSM will change from 0 to 1, 2, 3, 5 to a number of states, represented by state[2:0]. As the controller is in the process the FSM will switch from the state 0 to the state 1, the state 2 to the state 3, the state 5 to the state 5, etc., to the states that are represented by state[2:0]. The successful completion of the HDL generation, HDL classification, HDL verification and HDL completion is shown in these state changes. When the verification process is finished, all the pre-prescribed functional test cases should be "passed" with the signal pass in the simulation output, which is generated by the developed Verilog HDL. In the meantime, no fail signal is raised throughout the execution of the program showing that there are no syntax, compile and logical errors in the program after the adaptive error categorization and refinement process. An efficient framework for synthesizing functionally correct and synthesizable RTL is proposed in the paper and its output 'pass' is shown to be stable and high as demonstrated in the results.

V.CONCLUSION

The proposed IntelliRTL framework is an effective approach to leverage Large Language Models (LLMs) for the automatic generation of Register Transfer Level (RTL) code, along with an adaptive error classification and verification process. It decreases the debugging effort, the

number of unnecessary verifications, and the chance of error in the generated hardware design by automatically generating synthesizable Verilog HDL from natural language specifications and categorizing the errors as syntax, compilation, and logical errors before verification. For FPGA and ASIC applications, the iterative feedback method accelerates the entire development process, thereby ensuring the functional correctness of the development. The proposed system is highly scalable, efficient, and intelligent, providing a practical solution for modern Electronic Design Automation (EDA) tools in fast and effective hardware prototyping, design efficiency, and AI-aided digital system development. Additional enhancements to improve the accuracy and productivity of automated RTL generation could be incorporation of timing-aware optimization, power and resource analysis, SystemVerilog and VHDL support, and advanced multi-agent cooperation.

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